Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (cancel)

Claim 2 (currently amended): The method of claim [[1]] 17, wherein generating a low-~~interference~~ frequency clock further comprises generating an asymmetrical clock signal.

Claim 3 (currently amended): The method of claim [[1]] 17, ~~wherein the square wave clock has rising and falling edges and wherein~~ further comprising changing the duty cycle ~~further comprises~~ by changing ~~the~~ a position of the falling edge of ~~the~~ a square wave clock relative to ~~the~~ a position of the rising edge of the square wave clock.

Claim 4 (currently amended): The method of claim [[1]] 17, ~~wherein~~ further comprising minimizing ~~the~~ an nth-order harmonic associated with the low frequency clock signal ~~changes the magnitude of other harmonic~~.

Claim 5 (currently amended): The method of claim [[1]] 17, further comprising applying the low frequency clock signal in a digital receiver.

Claims 6-10 (cancel)

Claim 11 (currently amended): A clock generator, comprising:

[[A]] a high frequency clock/oscillator;

[[A]] a counter coupled to the clock/oscillator; and

[[A]] a controller coupled to receive an output of the ~~down~~ counter to generate a low frequency clock with an asymmetrical duty cycle.

Claim 12 (original): The clock generator of claim 11, wherein the clock oscillator generates an output at a high frequency relative to the low frequency clock.

Claim 13 (original): The clock generator of claim 11, wherein the counter is a down counter.

Claim 14 (original): The clock generator of claim 11, wherein the counter is a modulo counter.

Claim 15 (currently amended): The clock generator of claim 11, ~~wherein the symmetrical clock has rising and falling edges and~~ wherein the controller to change ~~changes~~ the position of ~~the~~ a falling edge of ~~the~~ a symmetrical clock relative to the position of ~~the~~ a rising edge of the symmetrical clock to obtain the asymmetrical duty cycle.

Claim 16 (currently amended): The clock generator of claim 11, wherein the controller ~~minimizes~~ to minimize the nth-order harmonic and ~~changes~~ change the magnitude of other harmonic.

Claim 17 (new): A method comprising:

obtaining a high frequency clock signal having a predetermined duty cycle; and

generating a low frequency clock signal from the high frequency clock signal at a changed duty cycle.

Claim 18 (new): The method of claim 17, further comprising changing the predetermined duty cycle based on a count value.

Claim 19 (new): The method of claim 18, further comprising triggering a falling edge of the low frequency clock signal when the count value is below a threshold.

Claim 20 (new): An apparatus comprising:

an oscillator to generate a first clock signal with a first duty cycle;

a counter coupled to the oscillator; and

a controller to generate a second clock signal with a second duty cycle formed by a first transition and a second transition, the second transition initiated when a value of the counter is at a predetermined value.

Claim 21 (new): The apparatus of claim 20, wherein the oscillator is at an intermediate frequency.

Claim 22 (new): The apparatus of claim 20, further comprising a digital portion.

Claim 23 (new): The apparatus of claim 22, wherein the oscillator and the digital portion are on a single substrate.

Claim 24 (new): The apparatus of claim 23, wherein the second clock signal to be provided to the digital portion.